

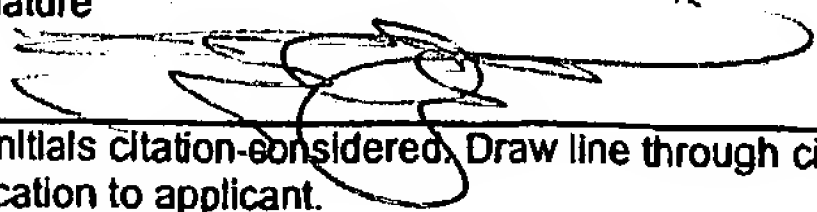
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Sheet 1 of 2

Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-317001	Application No. 09/760,509
	Applicant Gilbert Wolrich et al.		
	Filing Date January 12, 2001	Group Art Unit 2183	

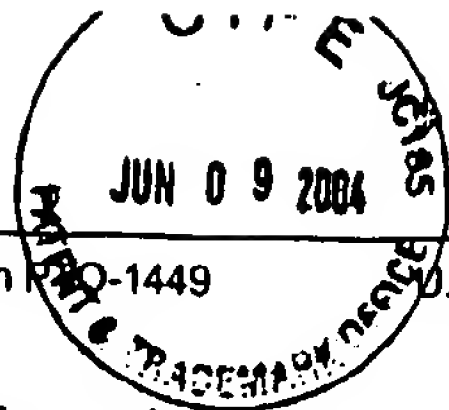
Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
B50	AA	WO 01/50679	07/12/2001	WIPO	—	—		
	AB	WO 01/50247	07/12/2001	WIPO	—	—		
	AC	WO 01/48619	07/05/2001	WIPO	—	—		
	AD	WO 01/48606	07/05/2001	WIPO	—	—		
	AE	WO 01/48599	07/05/2001	WIPO	—	—		
	AF	WO 01/48596	07/05/2001	WIPO	—	—		
	AG	WO 01/41530	06/14/2001	WIPO	—	—		
	AH	WO 01/16782	03/08/2001	WIPO	—	—		
	AI	WO 01/16770	03/08/2001	WIPO	—	—		
	AJ	WO 01/16769	03/08/2001	WIPO	—	—		
	AK	WO 01/16718	03/08/2001	WIPO	—	—		
	AL	WO 01/15718	03/08/2001	WIPO	—	—		
	AM	WO 97/38372	10/16/1997	WIPO	—	—		
	AN	WO 94/15287	07/07/1994	WIPO	—	—		
	AO	EP 0 809 180	11/26/1997	Europe	—	—		
	AP	EP 0 745 933	12/04/1996	Europe	—	—		
	AQ	EP 0 633 678	01/11/1995	Europe	—	—		
	AR	EP 0 464 715	01/08/1992	Europe	—	—		
	AS	EP 0 379 709	08/01/1990	Europe	—	—		
	AT	59111533	06/27/1984	Japan	—	—		

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
B50	AU	Agarwal et al., "April: A Processor Architecture for Multiprocessing," Proceedings of the 17 th Annual International Symposium on Computer Architecture, IEEE, pp. 104-114.
B50	AV	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
B50	AW	Chang et al., "A New Mechanism For Improving Branch Predictor Performance," IEEE, pp. 22-31 (1994).

Examiner Signature 	Date Considered 10/1/04
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

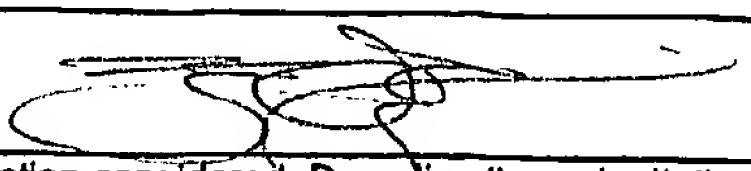
Substitute Disclosure Form (PTO-1449)

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	Applicant Gilbert Wolrich et al.		JUN 10 2004
	Filing Date January 12, 2001	Group and Unit 2183	Technology Center 2100

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
B50	AX	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
	AY	Farkas et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159.
	AZ	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AAA	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	ABB	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	ACC	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	ADD	Hennessy et al., "Computer Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482.
	AEE	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
	AFF	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21.
	AGG	Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998.
	AHH	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	AII	Mendelson et al., "Design Alternatives of Multithreaded Architecture," <i>International Journal of Parallel Programming</i> , vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193.
	AJJ	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
	AKK	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	ALL	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AMM	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998.
	ANN	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999.
	AOO	Vibhatavani et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
	APP	Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.
✓	AQQ	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

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